Exhibit D

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(54) **LOW TEMPERATURE PROCESS FOR FORMING INTER-METAL GAP-FILLING INSULATING LAYERS IN SILICON WAFER INTEGRATED CIRCUITRY**

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(52) **U.S. Cl.** **438/597**; 438/624; 438/937
(58) **Field of Search** 438/597, 624, 438/688, 687, 788, 937

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5,494,854		2/1996	Jain	437/195
5,679,606		10/1997	Wang et al.	437/195
5,728,631		3/1998	Wang	438/787
5,776,834		7/1998	Avanzino et al.	438/692
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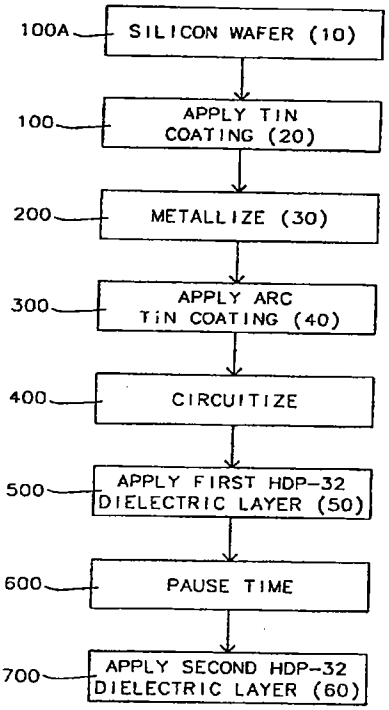
(57) **ABSTRACT**

This invention provides an in situ low temperature, two step deposition HDP-CVD process separated by a cooldown period, for forming an inter-metal dielectric passivation layer for an integrated circuit structure. Said process mitigating metal line defects such as distortion or warping caused by excessive heat generated during the etching/deposition process.

19 Claims, 2 Drawing Sheets



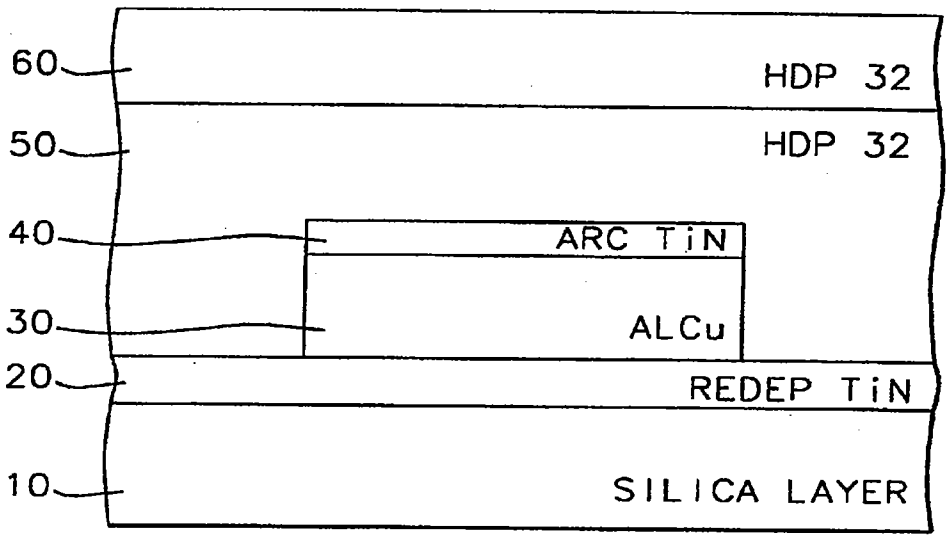

60
HDP 32
50
HDP 32
40
ARC TiN
30
ALCu
20
REDEP TiN
10
SILICA LAYER

FIG. 1

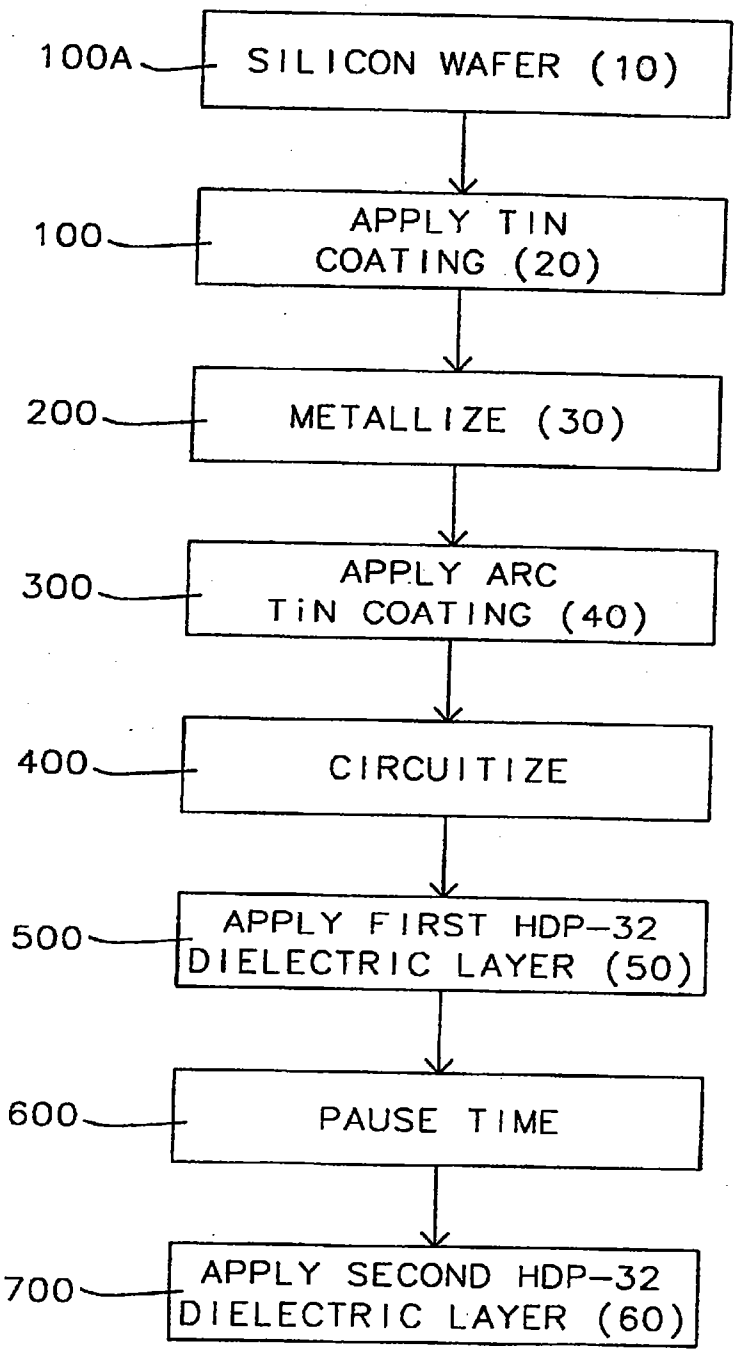

100A
SILICON WAFER (10)
100
APPLY TIN COATING (20)
200
METALLIZE (30)
300
APPLY ARC TiN COATING (40)
400
CIRCUITIZE
500
APPLY FIRST HDP-32 DIELECTRIC LAYER (50)
600
PAUSE TIME
700
APPLY SECOND HDP-32 DIELECTRIC LAYER (60)

FIG. 2

LOW TEMPERATURE PROCESS FOR FORMING INTER-METAL GAP-FILLING INSULATING LAYERS IN SILICON WAFER INTEGRATED CIRCUITRY

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a structure and process for fabricating an inter metal dielectric layer for integrated circuits interconnecting active and passive elements. More particularly, this invention relates to a structure and process for an inter metal dielectric layer formed using electron cyclotron resonance techniques employing high density plasma (HDP) and chemical vapor deposition (CVD) processes. A unique HDP-CVD two step deposition process is described that allows cooling between the steps thereby providing metal circuitry possessing no warping or distortion.

2. Description of the Prior Art

Integrated circuitry (IC) found in semiconductor chips are used in a variety of applications such as computers, televisions, and cars to name just a few. IC can combine millions of transistors onto a single crystal silicon chip to perform complex data and store data. There has been a strong desire and significant advancement in shrinking the dimensions of IC thereby providing a greater number of functions in an ever smaller volume. An excellent example is the hand held calculator which initially could only perform simple mathematical functions but now can perform the most sophisticated mathematical modeling or statistical analysis at a fraction of the cost of the older models. Cost and size reduction are major factors driving this technology and no end seems in sight. Historically, such process improvements have resulted in roughly a 13% annual decrease in the minimum feature widths achievable for transistors mid interconnections.

With miniaturization comes an increased complexity of interconnect wiring used to transport data across a chip, Complex wiring patterns that can include multiple layers can be found in IC. The problem of electronic isolation of the individual circuits becomes significant since designs must deal with intralayer as well as interlayer effects. Electronic isolation has been accomplished by providing insulating or dielectric material between the circuit neighbors. Obviously as the dimensions shrink there is greater challenge to maintain electronic isolation.

In the conventional formation of conductive lines in an integrated circuit, a metal layer is deposited and patterned by conventional lithography and etching techniques to form metal lines/patterns, thus creating an uneven surface on the semiconductor material. In addition to finding suitable dielectric materials that will provide adequate electronic isolation, miniaturization has also created the problem of providing techniques that will adequately apply the dielectric, insulating material. The problem faced in this regard is that although the distances between circuitry lines is decreasing, the height of the circuitry lines formed by photolithographic means is not decreasing. This creates a situation where the dielectric material must be applied between tall, closely spaced features. Features with this topography are said to have high aspect ratios (height/width) and understandably it becomes very difficult to fill between those features.

It is often desirable for the insulating layer to be so formed that the upper surface of the insulating layer is planar over an extended region, irrespective of whether individual portions of the upper surface overlie metal lines or contacts or the spaces between such lines/contacts. The formation of such an insulating layer having a planar upper surface is referred to as planarization. Those skilled in the art know this insulating layer by many terms, such as, dielectric layer, gap filling layer, and passivation layer. All these terms are used interchangeably in this document and therefore should be construed to have the same meaning. It is especially important to have a planarized surface when additional circuitry is to be stacked in a multilayer design.

Although various processes have been available for forming insulating (gap filling) layers, chemical vapor deposition (CVD) was preferred since it seemed to meet the stringent requirements of filling high aspect channels between individual circuit lines. However, the temperatures that were required to perform this technique can be very high and lead to warping, distortion or other defects to metal line circuitry. In order to provide for etching or sputtering the technique of plasma generation was used to enhance CVD. Plasma deposition processes are of interest in this regard, because they may be able to form insulating layers of silicon dioxide or silicon nitride at relatively lower temperatures. In particular, high density plasma (HDP) processes, such as electron cyclotron resonance (ECR) processes and induced coupling plasma (ICP) processes have been found to produce high-quality silicon dioxide and silicon nitride layers. High density plasma (HDP) when combined with CVD provides for an HDP-CVD process such as plasma enhanced chemical vapor deposition (PECVD) that allows both simultaneous deposition and sputtering and is performed in an electron cyclotron resonance (ECR) apparatus. With this tool it is possible to vary the ratio of deposition to sputter etching. And although this technique can indeed be used at a lower temperature than conventional CVD it still causes unacceptably high temperatures at the early stages of gap filling when low deposition/sputter ratios (typically less than 4) are necessary to fill the high aspect ratio channels. This is especially noted for metallic lines composed of aluminum and its alloys such as aluminum copper. Temperatures as high as 400° C. have been observed and at these temperatures significant distortion of the metal features and circuitry can be observed. Aluminum contacts are intolerant of processing temperatures greater than about 350–400 C because at such temperatures "hillocks" tend to form in aluminum or aluminum alloy features.

The conventional HDP CVD process described hereinabove has a major drawback in that the high density plasma (HDP) deposition of the ECR oxide insulating layer often damages the underlying circuit elements, especially metal lines. High density plasma (HDP) sources employ magnetic fields and microwave power to create chemically active plasmas, preferably at very low gas pressures. It is difficult to control the energy transferred to the reactant ions in the plasma deposition. The high density plasma (HDP) chemical vapor deposition (CVD) process (e.g., ECR) is an in situ sputtering and deposition process using an argon flow, high microwave power and RF power. The deposition and sputtering steps are performed sequentially and are repeated until the proper coverage is obtained. When the metal lines on the wafers are subjected to in situ sputtering this creates a damaging "antenna effect". The higher microwave power generates higher ion energy which increases the damage to the metal lines. The high power during the ECR oxidation process creates transconductance (i.e., gin) degradation due to the Fowler-Nordheim (F-N) tunneling stress. The defect that is readily observable is can be described as a hillock that protrudes above the surface of insulative layer and creating

concurrently a void in the wall between the opposite side of the metal line and its adjacent insulative layer.

Therefore, there is still a need to create a structure and process whereby the damage to semiconductor devices, e.g., metal lines, from high density plasma (e.g. HDP and ECR) deposition of insulating layer is significantly reduced or eliminated.

Jain in U.S. Pat. No. 5,494,854, describes a gap-fill dielectric layer useful conductor lines that have low and high aspect channels separating the lines. In this invention HDP is used to assist in forming a dielectric layer that is specifically planarized in areas that cover high aspect conductor lines but necessarily between low aspect conductor lines. Furthermore, Jain does not teach the benefit of a pause time during the HDP process.

Wang et al. in U.S. Pat. No. 5,679,606, describe a process for forming a planar dielectric layer over metal lines using an in situ multi-step ECR deposition process. The invention describes forming a series of coatings that are alternating "gap filling" and "protective" dielectric which coat the metal lines and the substrate. The initial "protective" coating is formed using the ECR process and employs no argon flow during this step. The "gap filling" coating is now prepared also using the ECR process but now in this case with an argon gas flow. The "gap filling" process simultaneously etches and deposits. However, it etches mainly on the topmost surface of the metal lines, in doing so, it reduces the aspect ratio of the channels thereby ultimately facilitating in planarization. Although a multi-step process is described by Wang et al., no mention is made of having a pause time between the steps, nor is any concern expressed about cooling the wafer during such a time period.

Wang in U.S. Pat. No. 5,728,631, describes a method of forming a low capacitance dielectric layer with the use of ECR. The layer is composed of silicon dioxide but is not uniform, since it is the expressed object of the invention to have closed voids of air between the metallic circuitry lines. Although Wang notes that changes to the etch-to-deposition rate must be altered during the process in order to obtain closed voids, no mention is made of having a pause time allowing cooling to occur as required by the present invention.

Avanzino et al. in U.S. Pat. No. 5,776,834 disclose a method of forming a planarized dielectric layer covering metal layers, said dielectric layer contains voids within the high aspect ratio channels (e.g. close metal line neighbors). The process comprises first coating a nonconformal source with a poor step function in order to generate the void. Then the nonconformal material is etched either simultaneously or sequentially along with deposition to fill the remaining gaps with void free insulating material. However, Avanzino et al. do not disclose a pause time between the two stages of the process and further make no mention of a cooling process during this time period.

Yao et al. in U.S. Pat. No. 5,814,564, teach a planarization method for a spin-on-glass layer over a dielectric layer that is applied by use of the HDP-CVD process. The planarization method involves a six step etchback process of the SOG layer to provide a planar upper surface. No mention is made of a pause time during the formation of the dielectric layer nor to any concern to provide cooling during the deposition/etching process.

Matsuo et al, U.S. Pat. No. 4,962,620, Goto, U.S. Pat. No. 4,778,620, and Maydan, U.S. Pat. No. 4,962,063 show methods and equipment for ECR deposition of dielectric layers. The article "Improved Sub-micron Inter-metal Dielectric Gap-filling Using TEOS/OZONE APCVD" by E. J. Korczyski et al, published in the Microelectronics, January 1992 pp. 22–27 provides a comparison of ECR and TEOS/03 planarization methods.

Although considerable progress has been made in finding methods to reduce the metal line spacing on semiconductor wafers such as silicon single crystals, a problem still exists that manufacturing processes for the formation of the insulating layer can cause failures due to excessive heating of the metal lines. The most common failure is metal line distortion that manifests itself as reliability problems. This specific distortion problem is observed with the formation of unwanted "hillocks" that bulge out from the top of the metal line and are exposed on the surface of the insulator (dielectric) layer. This defect is especially noted in CVD processes but still problematic in one-step HDP-CVD processes where temperatures can still rise above 400° C. during the deposition process.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method of forming a void-free inter metal dielectric/insulative layer.

It is another object of the present invention to provide a method of forming an inter-metal dielectric layer that will reduce the damage (specifically metal distortion) to conductive lines caused by HDP-CVD of silicon oxide insulating layers.

It is still another object of the present invention to utilize an in situ simultaneous deposition and sputtering (etching) HDP-CVD process to generate insulation layers for metal lines on semiconductor wafers.

It is yet another object of the present invention to provide a good oxide film protection to the metal lines without any metal line exposure to PECVD nitride film by using lower HDP CVD temperature.

It is yet another object of the invention to provide a gap filling, insulation layer that can readily be planarized to allow additional integrated circuitry be formed in layers thereon.

It is another object of the present invention to provide wafer boards for use as 0.35 micron logic boards and 0.25 micron DRAM.

Still another object of the present invention is to improve the throughput of the HDP CVD process for insulating metallurgical lines and thereby provide a low cost process.

In accordance with the above objectives, this invention provides an in situ low temperature two step process for forming an inter-metal dielectric layer of an integrated circuit structure reducing damage caused by excessive heat generated during electron cyclotron resonance deposition of insulating layers.

The inventive process relates to manufacturing insulating inter-layers between closely spaced metallurgy lines on a semiconductor substrate, such as silicon, having line spacing on the order of 0.25 micron or less. During the course of designing these articles it was observed that a defect known as a "hillock" would occasionally form. This was unexpected because the prior art had taught that manufacturing these insulating layers using techniques like HDP-CVD should be capable of manufacturing the insulative layer at low temperatures thereby avoiding high temperatures that could cause metal line distortion. However, for closely spaced lines, on the order of 0.25 micron or less, the process requires low deposition/etching ratio to fill the narrow channels and essentially simultaneous etching and deposition. This regime causes high temperatures to be generated.

It was determined that neither titanium nitride protective (seed) nor passivation (insulative) layer thickness would alleviate the defect. Furthermore, RF power did not seem to be an important factor in defect production. It was unexpectedly discovered that by increasing inert gas backside pressure and having a cooling period during the deposition process essentially eliminated the defect from forming.

Therefore, the inventive process comprises insulating these lines by a two step HDP-CVD process wherein each step simultaneously deposits and etches a dielectric material such as silicon dioxide. The first step is performed with a low deposition-to-sputtering ratio (D/S) of 2 to 4 and Helium backpressure of 8 inner and 10 outer Torr. Subsequently there is a period of time where no deposition or etching is allowed and the wafer is subjected to cooling by applying a stream of inert gas to the backside of the wafer. After this treatment the deposition/sputtering is resumed with a D/S of 4 to 6 and a Helium backpressure of 6 inner and 10 outer Torr. In this manner the temperature of the metallurgy lines is maintained below a point that would cause distortion of the lines, specifically no "hillocks" are formed.

BRIEF DESCRIPTION OF THE DRAWINGS

The drawings show the following:

FIG. **1** is a schematic cross sectional view of the manufactured semiconductor wafer as disclosed in the present invention.

FIG. **2** is a flow chart describing the critical manufacturing steps to produce the wafer schematically shown in FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the present invention, the dielectric layer, also referred to as an insulative, gap filling or passivation layer, is preferably formed of undoped silicon dioxide glass (USG). Insulating layers composed of this type of material can be applied to semiconductor wafer surfaces using electron cyclotron resonance (ECR) plasma deposition as described in U.S. Pat. No. 4,962,063, Maydan et al. and is hereby incorporated by reference.

In one preferred embodiment the process begins with deposition of a uniform seed layer (**20**) of titanium nitride (TiN) on the lateral surfaces of the silicon substrate (**10**). This layer is approximately 100 to 1000 A in thickness. The preferred thickness of the titanium nitride layer is in the range between about 300 to 800 A and more preferably about 500 A. This step is optional and other embodiments of the present invention do not require this treatment.

Closely spaced metallurgy lines (**30**) are formed on a semiconductor substrate (e.g., single crystal silicon) or the optional TiN layer, typically by photolithographic means. In this manner line width and line spacing of <0.25 micron are achievable and further used in the present invention. The height of the lines can be between 0.3 microns and 1.2 microns. The preferred thickness of the metal lines is about 0.8 micron, therefore the aspect ratio of these metallurgy lines will typically be >2. The metallurgy lines can be composed of any metallic substance that can transmit electrical current, examples include aluminum and its alloys, copper and its alloys, and nickel and its alloys. Preferred metallurgy include aluminum and its alloys. The most preferred metal composition is aluminum:copper (95:5).

Optionally, a top coat seed layer (**40**) of titanium nitride (TiN) is deposited on the uppermost surface of the metal substance prior to circuitization. This layer is approximately 100 to 500 A in thickness and is known in the industry as an "antireflective coating" (ARC). The purpose of the ARC is to reduce the reflective light from the stepper during the photolithographic process. Furthermore, the ARC can also reduce the electromigration of metal lines.

The preferred thickness of the titanium nitride layer (**40**) is in the range between about 150 to 400 A and more preferably about 250 A.

Subsequently, the seed layer (**20**) and the ARC TiN (**40**) covered metallurgy lines (**30**) are encapsulated with stoichiometric, high quality silicon dioxide passivation layers (**50** and **60**). The passivation layers are formed by an HDP-CVD technique utilizing two separate in situ, simultaneous deposition and sputtering steps separated by a cooldown period. The specific conditions for the deposition and sputtering steps provide void-free gap-filling between the metal structures. The first deposition/sputtering step is characterized by a low D/S ratio of about 3.2 while the second D/S ratio is characterized by a high value of about 6. The D/S ratio is defined as:

$$D/S=\{(\text{net deposition rate})+(\text{blanket sputtering rate})\}/(\text{blanket sputtering rate}).$$

A helium backpressure of 6–8 Torr (inner) and 10–12 Torr (outer) is used during this process and the RF power bias is about 3000 to about 4000 W. Preferred wattage is 3500 W. The first deposition step takes approximately 70–90 seconds.

The passivation layers or insulation layers (**50** and **60**) can be composed of a dielectric material such as a Group IV material oxide, nitride or combination thereof. Specifically, silicon is the preferred Group IV material. These materials can also be doped with low levels of boron materials to create a positive doped insulation or phosphorous materials to generate a negative doped insulation. The oxide or nitride insulation are formed in situ and it is desirable that they do not form solid masses until they precipitate on the surface of the metal lines or newly deposited passivation layer. In this manner smooth coatings are generated. As mentioned supra, this process is known as deposition and is performed using an ECR apparatus with specific requirements for argon flow and RF power.

Occurring simultaneously with deposition is etching or sputtering of the newly deposited passivation layer. The etch rate is a function of surface angle as well as the argon flow and RF power.

The first passivation layer (**50**) is formed over the optional protective layer (**40**). The HDP-CVD process is set to so that the passivation layer fills in between the lines, but does not etch through the protective layer (**40**). The passivation layer (**50**) does not expose the metallurgy lines. The HDP-CVD parameters are set such that the passivation layer (**50**) can fill between closely spaced metallurgy lines without forming voids.

In this manner of deposition/sputtering the ratio is selected between a value of about 2 to about 4 and the passivation layer (**50**) is formed in the range between about 5000 to 10,000 A., more preferably about 7500 A, and most preferably 5000 A. During this time the wafer and the metal lines are being undesirably heated as a by product of the deposition/sputtering process. The heating raises the temperature of the wafer and the metal lines essentially monotonically with time so that the thicker the layer deposited the higher the temperature of the metal lines (**30**). Above a critical temperature the metal lines will become distorted as the metal lines (**30**) essentially flow through the protective

layer (40) and cover a portion of the newly formed passivation layer (50). Therefore, the maximal thickness of the passivation layer (50) in this step is dictated by the temperature of the metal lines (30). As mentioned supra, typically the thickness of the passivation layer (50) at this point in the process will be approximately 5000 to 6000 A.

The overall process flow for the invention is depicted in FIG. 2 as a flow diagram.

A key inventive feature of the process in the present invention is the cooldown period between the first deposition/sputtering step described above and a second deposition/sputtering step described hereinbelow. The cooldown process employs argon or helium gas applied to the wafer backside for a period of about 10 seconds. By performing the process in this manner the temperature of the metal lines never exceeds about 350 C, well below the melting point of the metal lines. The protective layer so formed does not attack the metallurgy lines and shields the metallurgy lines from attack from the subsequent ECR depositions of "gap filling layers".

An alternative embodiment of the present invention replaces the cooldown period with a "vacuum break", however this step requires approximately 120 seconds and therefore is longer and less desirable than the cooldown period of approximately 10 seconds.

The cooling period is required in order to continue the process of increasing the thickness of the passivation layer while still maintaining temperatures of the metal lines that will not cause distortion defects. It is highly desirable to cool the wafer and the metal lines using an in situ process so that the wafer need not be disturbed. This is provided by applying an inert gas under high flow to impinge the backside of the wafer. Inert gas such as argon or helium are typically utilized for this purpose but it is within the scope of the invention that other gases such as could be used. The cooling process is selected to cool the wafer to such a point the remaining deposition/sputtering process will not cause damage to the metal lines. Typically this yields cooling times on the order of about ten seconds. Longer times are allowable but no obvious benefit is derived.

An alternative embodiment of the present invention replaces the cooldown period with a "vacuum break", however this step requires approximately 120 seconds and therefore is longer and less desirable than the cooldown period of approximately 10 seconds.

Following the cool down phase, the process of deposition/sputtering is resumed. Since the first deposition of the passivation layer was not conformal due to the low deposition/sputter value, the covered metal lines now have an aspect ratio of approximately 1. For the second phase of deposition the deposition/sputtering ratio can now be increased from about 5 to about 7. Under these conditions it is possible to fill in the channels between the lines and further deposit material on the upper surface so that an additional 3000 to about 7000 A is deposited on the wafer. The preferred thickness for the second deposition is 5000 A. The total thickness of the two combined passivation layers covering the wafer is approximately 8000 to about 13000 A whether or not there is a metal line beneath the surface, therefore at this point in the process the passivation layer is essentially planar. The preferred thickness for the two combined stages is 10,000 A.

The process is performed using helium backside pressure of 8 Torr (inner) and 10 Torr (outer) and a bias RF wattage of between 2500 to about 3500 W. Preferred wattage is approximately 2800 W. This phase of the process takes approximately 40 to 50 seconds. It is within the scope of this invention that the dielectric material deposited be the same or different than that used in the first deposition process, optional materials are described supra in the section discussing the first deposition process.

Optionally a capping layer can be applied to the top surface of the passivation layer should that be desired. Following the optional capping layer additional metallurgy lines can be formed on the uppermost surface.

WORKING EXAMPLES

Example 1

Process for Forming the First Insulative Layer (50); Step 500 in the Flow Diagram.

The first dielectric layer (50) prior to the cooling period is formed of silicon dioxide and is formed using electron cyclotron resonance (ECR) plasma deposition as described in U.S. Pat. No. 4,962,063, Maydan et al. Oxygen should be fed into the plasma formation chamber at a rate of from about 80 standard cubic centimeters per minute (sccm) to about 150 sccm; and silane into the deposition chamber, at a rate of from about 30 sccm to about 80 sccm; and argon at a rate between about 80 to 140 sccm and more preferably about 110 sccm; while maintaining the temperature in the deposition chamber at from about 25° C. to about 400° C.; and a pressure ranging from about 2 to about 15 Millitorr. A plasma power level of from about 1000 to about 2000 Watts should be used.

Example 2

Good quality HDP may be deposited, for example, in an Applied Materials deposition chamber using the following procedure: a wafer (containing the substrate) is mounted in the chamber such that backside helium cooling may be used to control temperature; the chamber is then evacuated to 240 Millitorr, and a mixture of 120 sccm oxygen and 110 sccm argon are supplied to the chamber; 1300 W of source RF power are used to create a plasma (which also heats the wafer), and the temperature of the wafer is maintained at 310 to 320 C. by backside cooling; after 10 to 15 seconds of operation, 150 sccm silane is also introduced into the chamber, causing a silane oxide to deposit on the wafer; after 10 to 15 seconds of operation, 2800 W of bias power is applied to initiate dc-bias sputtering; at this point, net deposition rate drops to 1500 to about 2500 A./sec, with roughly a 4:1 deposition to sputter ratio. At this rate, an excellent quality oxide may be deposited.

It should be noted that the invention as described hereinabove depicts a metallurgical circuitry of lines (30) that are affixed to the silicon substrate (10), however, the invention is not limited to this design, in fact, this invention can be employed for metallurgical circuitry on any layer within a multi-layered integrated circuit design. Furthermore, the invention can be practiced on multiple layers within a multilayered integrated circuit design.

The in situ two-step deposition process (Steps 500, 600, 700 of FIG. 2) of the invention forms dielectric oxide layers between closely spaced lines without damaging the metallurgy lines. The process is inexpensive, simple to implement and increases device yields.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and the scope of the invention.

What we claim is:

1. A process for forming an inter metal protective layer between closely spaced metallurgy lines on a semiconductor surface comprising the steps of:

a) providing a semiconductor substrate with closely spaced metallurgy lines thereon;

b) encapsulating said substrate and said metallurgy lines with a first passivation layer; said first passivation layer formed by an HDP-CVD technique using high density plasma chemical vapor deposition;

c) stopping said encapsulating process;

d) impinging inert gas to backside of said substrate for the purpose of cooling said passivation layer and said metallurgy lines; and

e) resuming said encapsulation process on said first protective layer from step (b) to generate a second passivation layer.

2. The process as recited in claim 1 wherein said step (b) HDP-CVD technique is performed with a deposition to sputter ratio of about 2 to about 4.

3. The process as recited in claim 1 wherein said step (d) HDP-CVD technique is performed with a deposition to sputter ratio of about 5 to about 7.

4. The process as recited in claim 1 wherein said step (c) stopping and said step (d) impinging inert gas is performed to sufficiently cool said first and second passivation layers and said metallurgy lines so that no warping or distortion of the metallurgy lines occurs during said step (e).

5. The process as recited in claim 4 wherein said steps (c) and (d) are performed simultaneously.

6. The process as recited in claim 1 wherein said stopping is for a minimum of about 10 seconds.

7. The process as recited in claim 1 wherein said metallurgy lines in said steps (a) through (e) are not heated above about 350° C.

8. The process as recited in claim 1 wherein said inert gas is selected from the group consisting of argon and helium.

9. The process as recited in claim 1 wherein the distance between said closely spaced metallurgy lines is less than 0.4 microns.

10. The process as recited in claim 1 wherein said metallurgy lines has an initial aspect ratio of at least 2.

11. The process as recited in claim 1 wherein at the end of said step (b) encapsulated metallurgy lines has an aspect ratio of about 1.

12. The process as recited in claim 1 wherein said metallurgy lines comprise aluminum and its alloys.

13. The process as recited in claim 11 wherein said aluminum alloy comprises copper/aluminum.

14. The process as recited in claim 1 wherein said first and second passivation layer independently comprises Group IV oxides or nitrides and mixtures thereof.

15. The process as recited in claim 12 wherein said Group IV oxides comprise silicon oxide.

16. The process as recited in claim 12 wherein said Group IV nitrides comprise silicon nitride.

17. The process as recited in claim 1 wherein:

said step (b) encapsulation process is performed using Bias RF 2800 W and a backside inert gas pressure of about 6 Torr in order to generate said first protective layer thickness of about 5000 Angstrom, and said step (d) encapsulation process is performed using Bias RF 2800 W and a backside inert gas pressure of about 10 Torr in order to generate said second protective layer thickness of about 5000 Angstrom.

18. The process as recited in claim 1 wherein:

said step (b) encapsulating process is performed using Bias RF 2800 W and a backside inert gas pressure of about 8 Torr in order to generate said first passivation layer thickness of about 5000 Angstrom, and

said step (d) encapsulation process is performed using Bias RF 3500 W and a backside inert gas pressure of about 10 Torr in order to generate said second passivation layer thickness of about 5000 Angstrom.

19. The process as recited in claim 1 further comprising the step of: f) applying, prior to said step (a), a TiN antireflective coating layer to an outer surface of said metallurgic lines for the purpose of protecting said metallurgic lines from sputtering, said TiN layer having a thickness of 250 Angstrom.

* * * * *

Exhibit E

US006174797B1

(12) **United States Patent**
Bao et al.

(10) **Patent No.: US 6,174,797 B1**
(45) **Date of Patent: Jan. 16, 2001**

(54) **SILICON OXIDE DIELECTRIC MATERIAL WITH EXCESS SILICON AS DIFFUSION BARRIER LAYER**

(75) Inventors: **Tien-I Bao; Syun-Ming Jang**, both of Hsin-Chu (TW)

(73) Assignee: **Taiwan Semiconductor Manufacturing Company**, Hsin-Chu (TW)

(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **09/435,678**

(22) Filed: **Nov. 8, 1999**

(51) **Int. Cl.**[7] **H01L 21/4763**
(52) **U.S. Cl.** **438/624**; 438/643; 438/653
(58) **Field of Search** 438/624, 706, 438/656, 789, 627, 643, 653; 205/666, 667; 216/2, 67, 74, 76, 79

(56) **References Cited**

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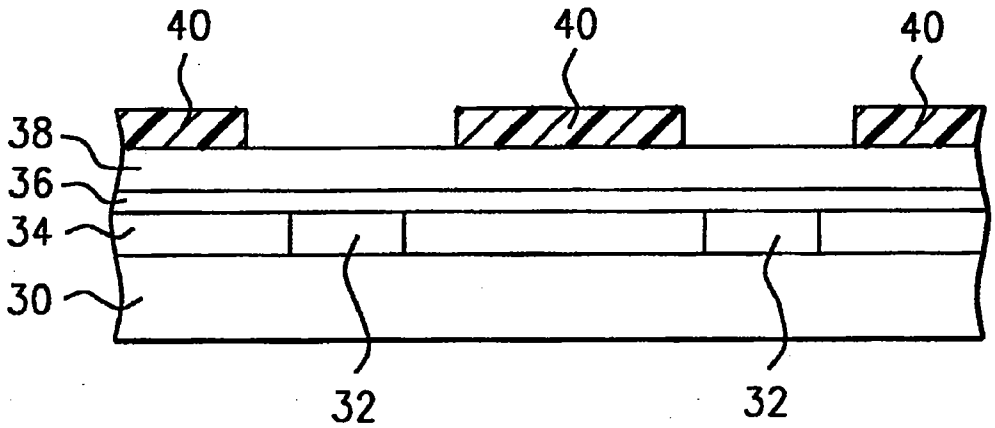
(74) *Attorney, Agent, or Firm*—George O. Saile; Stephen B. Ackerman

(57) **ABSTRACT**

A method for forming upon a substrate employed within a microelectronics fabrication a first dielectric layer, an intermediate diffusion barrier dielectric layer and a conductor layer which comprise an inter-level metal dielectric (IMD) layer with attenuated diffusion between the dielectric layers and conductor layer. There is first provided a substrate employed within a microelectronics fabrication. There is then formed upon the substrate a patterned microelectronics layer. There is then formed over the substrate a first dielectric layer. There is then formed over the substrate a diffusion barrier dielectric layer. There is then formed over the substrate a conductor layer to complete an inter-level metal dielectric (IMD) layer with attenuated inter-diffusion between the dielectric layers and conductor layer.

18 Claims, 4 Drawing Sheets



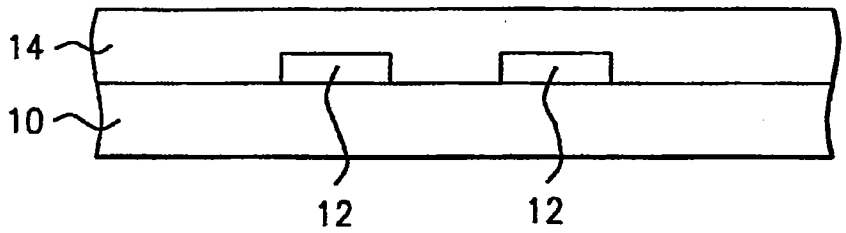


FIG. 1

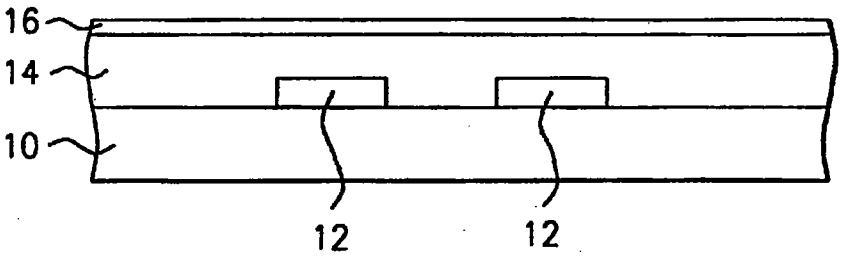


FIG. 2

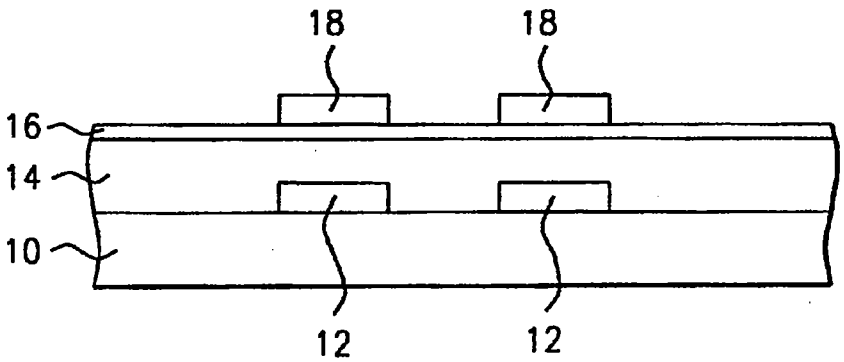


FIG. 3

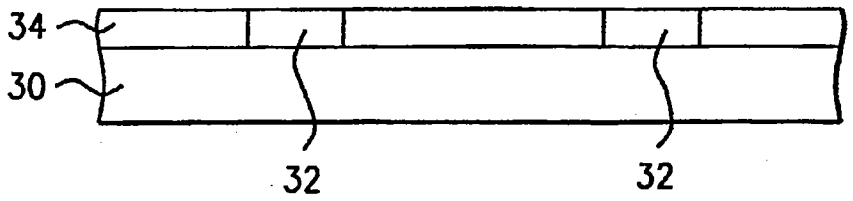


FIG. 4

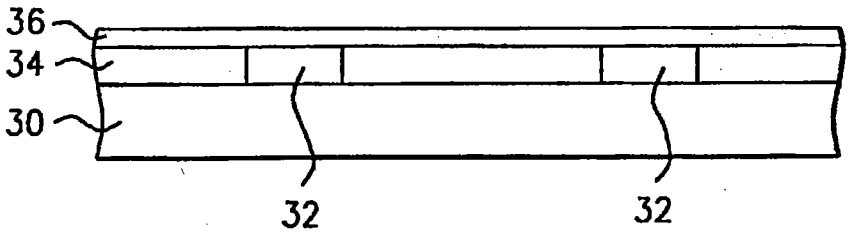


FIG. 5

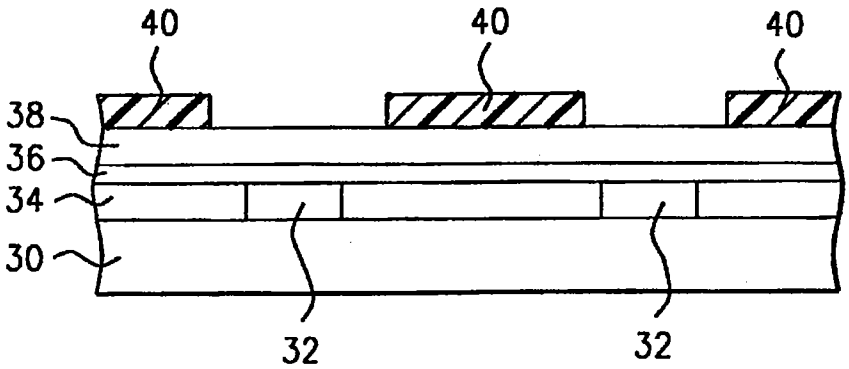


FIG. 6

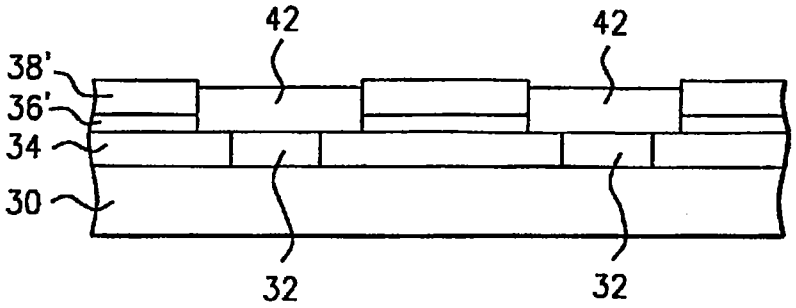


FIG. 7

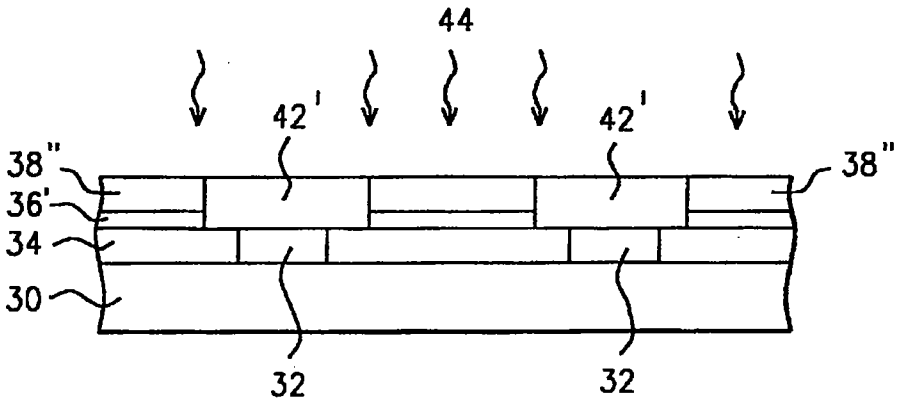
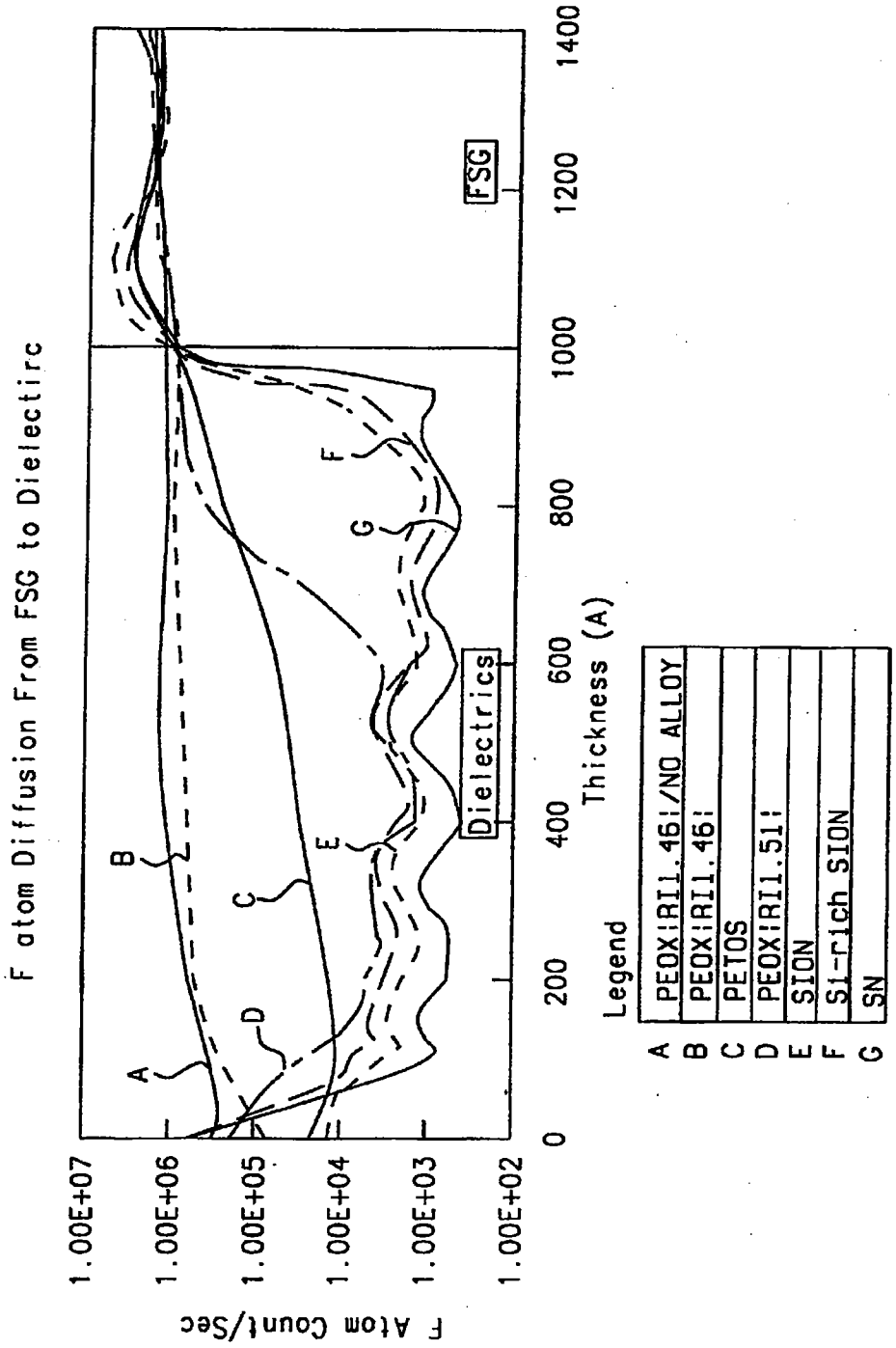


FIG. 8


F atom Diffusion From FSG to Dielectirc
F Atom Count/Sec
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1.00E+06
1.00E+05
1.00E+04
1.00E+03
1.00E+02
0
200
400
600
800
1000
1200
1400
Thickness (A)
FSG
Dielectrics
A
B
C
D
E
F
G
Legend
PEOX!RI1.46!/NO ALLOY
PEOX!RI1.46!
PETOS
PEOX!RI1.51!
SION
Si-rich SION
SN

FIG. 9

SILICON OXIDE DIELECTRIC MATERIAL WITH EXCESS SILICON AS DIFFUSION BARRIER LAYER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to the field of microelectronics fabrications, and more particularly to the field of dielectric layers employed within microelectronics fabrications.

2. Description of the Related Art

In order to fabricate microelectronics devices it is necessary to employ layers of dielectric material to electrically insulate patterned conductor material layers which serve to interconnect the devices in the microelectronics fabrication. As microelectronics devices have become more complex and densely populated, the requirements on the conductor and dielectric layers have become more stringent. The need to minimize power requirements and resistive losses has led to the employment of materials with higher electrical conductivity such as copper, for example. These conductor layers are often fabricated in complex and sophisticated configurations such as inlaid or damascene designs in order to maintain surface planarity in multi-layer structures. The conductor layer may act as a diffusion barrier towards substances emanating from other layers or, conversely, the conductor layer may require a barrier layer to protect it from deleterious substances or to protect other layers from itself.

Dielectric materials which are useful for formation of dielectric layers employed within microelectronics fabrications often are desired to have low dielectric constants to increase circuit performance. Such low dielectric constant materials as organic polymer dielectric materials or fluorine-doped silicon containing glass dielectric materials are commonly employed. Likewise, the increased circuit density and complexity has also led to multiple conductor layers and dielectric layers being fabricated into inter-level metal dielectric (IMD) layers to be able to accommodate all the requirements of increased circuit density and interconnectability. Although methods and materials are available which are satisfactory for these purposes in general, the employment of multi-level conductor layers and low dielectric constant dielectric layers is not without problems.

For example, the dielectric material selected for optimum electrical performance may require a method of formation or a composition which is incompatible with the physical or chemical properties of the conductor material with which the dielectric layer is in intimate contact.

It is thus towards the goal of forming a dielectric layer with an adjacent dielectric diffusion barrier material to protect conductor materials such as copper that the present invention is generally directed.

Various methods have been disclosed for forming conductor layers such as copper and a diffusion barrier layer upon an adjacent dielectric layer to attenuate damage to conductor material from nearby diffusing deleterious species.

For example, Cheung et al., in U.S. Pat. No. 5,785,236, disclose a method for forming aluminum or gold wire bonds to copper bonding pads. The method employs copper bonding pads supported within an interlayer dielectric which may be composed of silicon nitride,

Further, Bhattacharya et al., in U.S. Pat. No. 5,811,870, disclose a method for forming an anti-fuse structure which can be transformed from a non-conductive to a conductive state by application of a voltage across a two-layer insulator. The two-layer structure employs a dielectric layer and an injector layer. The latter employs a silicon-rich silicon oxide or silicon nitride layer.

Yet further, Cleeves et al., in U.S. Pat. No. 5,830,804, disclose a method for forming an encapsulated dielectric layer. The method employs a disposable post material over which is formed a dielectric layer which completely surrounds the post material. A second and third dielectric layer are formed over the encapsulated post and then a portion of the third layer is selectively removed to reveal the disposable post, which is then removed to form an opening in the dielectric layers.

Yet further still, Boeck et al., in U.S. Pat. No. 5,880,018, disclose a method for forming an inter-level metal dielectric (IMD) layer with reduced cross-talk. The method employs a selective placement of a low dielectric constant dielectric material with a dielectric constant equal or less than 3.5 within the IMD layer, and employs various conductor materials.

Finally, Wong et al., in U.S. Pat. No. 5,946,601, disclose a method for forming a layer which can function as a liner or barrier layer to separate a low dielectric constant dielectric layer from surrounding metal layers. The method employs a layer of amorphous hydrogenated carbon nitride and amorphous carbon nitride to separate a low dielectric constant dielectric material containing fluorine from a metal layer.

Desirable in the art of microelectronics fabrication are additional methods for forming an inter-level metal (IMD) layer within which is formed a diffusion barrier dielectric layer and employing conductor layers which are sensitive to corrosion such as copper.

It is towards this goal that the present invention is generally and more specifically directed.

SUMMARY OF THE INVENTION

A first object of the present invention is to provide a method for forming upon a substrate employed within a microelectronics fabrication a diffusion barrier dielectric layer intermediate between a dielectric layer and a conductor layer to attenuate inter-diffusion between the dielectric layer and the conductor layer

A second object of the present invention is to provide a method in accord with the first object of the present invention, where the diffusion barrier dielectric layer is formed employing silicon-rich silicon oxide dielectric material deposited employing plasma enhanced chemical vapor deposition (PECVD) upon fluorine-doped low dielectric constant dielectric material.

A third object of the present invention is to provide a method in accord with the first object of the present invention and the second object of the present invention, where there is formed an inter-level metal dielectric (IMD) layer comprising a layer of fluorine-doped low dielectric constant dielectric material, an intermediate silicon rich silicon oxide dielectric diffusion barrier layer and a copper conductor layer.

A fourth object of the present invention is to provide a method in accord with the first object of the present invention, the second object of the present invention and the third object of the present invention, where the method is readily commercially implemented.

In accord with the objects of the present invention, there is provided a method for forming upon a substrate employed

within a microelectronics fabrication a dielectric layer, an intermediate diffusion barrier dielectric layer and a conductor layer which constitute an inter-level metal dielectric (IMD) layer with attenuated inter-diffusion. To practice the invention, there is provided a substrate employed within a microelectronics fabrication. There is formed upon the substrate a patterned microelectronics layer and a dielectric layer. There is then formed over the substrate a silicon-rich silicon oxide dielectric layer employing plasma enhanced chemical vapor deposition (PECVD) which acts as a diffusion barrier. There is then formed over the diffusion barrier dielectric layer a copper conductor layer to complete an inter-level metal dielectric (IMD) layer with attenuated inter-diffusion between the dielectric layers and the conductor layer.

The present invention may be applied to substrates employed within microelectronics fabrications including integrated circuit microelectronics fabrications, charge coupled device microelectronics fabrications, solar cell microelectronics fabrications, radiation emitting microelectronics fabrications, ceramics substrate microelectronics fabrications and flat panel display microelectronics fabrications.

The present invention uses methods and materials which are known in the art of microelectronics fabrications, but in a novel order and fashion in order to achieve the results of the present invention. Therefore the present invention is readily commercially implemented.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the present invention are understood within the context of the Description of the Preferred Embodiments, as set forth below. The Description of the Preferred Embodiment is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

FIG. 1, FIG. 2, FIG. 3 are a series of schematic cross-sectional diagrams illustrating the formation upon a substrate employed within a microelectronics fabrication in accord with a general embodiment of the present invention of a dielectric layer with an intermediate diffusion barrier dielectric layer and a conductor layer to form an inter-level metal dielectric (IMD) layer with attenuated interdiffusion.

FIG. 4, FIG. 5, FIG. 6, FIG. 7, and FIG. 8 are a series of schematic cross-sectional diagrams illustrating the formation upon a semiconductor substrate employed within an integrated circuit microelectronics fabrication, in accord with a more specific embodiment of the present invention, of a fluorine containing low dielectric constant dielectric layer, an intermediate silicon-rich silicon oxide diffusion barrier dielectric layer and a copper conductor layer, to form an inter-level metal dielectric (IMD) layer with attenuated diffusion of fluorine species.

FIG. 9 is a graph showing the diffusion of fluorine species within various dielectric materials.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides a method for forming an inter-level metal dielectric (IMD) layer upon a substrate employed within a microelectronics fabrication wherein the dielectric layer has formed an intermediate diffusion barrier dielectric layer between it and the conductor layer, with attenuated inter-diffusion.

First Preferred Embodiment

FIG. 1 to FIG. 3 illustrate the formation of an inter-level metal dielectric (IMD) layer having an intermediate diffusion barrier dielectric layer between it and the conductor layer in accord with a general embodiment of the present invention which constitutes a first preferred embodiment of the present invention. FIG. 1 is a schematic cross-sectional diagram of a substrate at an early stage in its fabrication in accord with the first preferred embodiment of the present invention.

Shown in FIG. 1 is a substrate **10** over which is formed a patterned microelectronics layer **12**. Formed over the substrate is a dielectric layer **14**.

With respect to the substrate **10** shown in FIG. **1**, the substrate **10** is formed of material selected from the group including but not limited to microelectronics conductor material, microelectronics semiconductor material and microelectronics dielectric material. The substrate **10** may be the substrate itself employed within a microelectronics fabrication, or alternatively the substrate **10** may be any of several layers of microelectronics material formed over the substrate. Preferably the substrate **10** is a semiconductor substrate employed within a microelectronics fabrication selected from the group consisting of integrated circuit microelectronics fabrications, charge coupled device microelectronics fabrications, solar cell microelectronics fabrications, ceramic substrate microelectronics fabrications, optoelectronics microelectronics fabrications and flat panel display microelectronics fabrications.

With respect to the patterned microelectronics layer **12** shown in FIG. **1**, the patterned microelectronics layer **12** is formed employing materials selected from the group consisting of microelectronics conductor materials, microelectronics semiconductor materials and microelectronics dielectric materials, deposited and patterned employing methods as are well known in the art of microelectronics fabrication. Preferably the patterned microelectronics layer **12** is a microelectronics conductor layer.

With respect to the dielectric layer **14** shown in FIG. **1**, the dielectric layer **14** is a layer of dielectric material formed employing methods including but not limited to chemical vapor deposition (CVD), plasma assisted chemical vapor deposition (PECVD) methods, high density plasma chemical vapor deposition (HDP-CVD) methods, sub-atmospheric pressure thermal chemical vapor deposition (SACVD) methods, low pressure chemical vapor deposition (LPCVD) methods, spin-on-glass (SOG) methods and spin-on-polymer (SOP) methods. Preferably the dielectric layer **14** is formed employing a low dielectric constant dielectric material such as fluorine-doped silicon containing glass (FSG) dielectric material or, alternatively, fluorine-doped carbon containing dielectric material.

Referring now more particularly to FIG. **2**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is shown in FIG. **1** in accord with the first preferred embodiment of the present invention. Shown in FIG. **2** is a microelectronics fabrication otherwise equivalent to the microelectronics fabrication shown in FIG. **1**, but where there has been formed over the substrate a diffusion barrier dielectric layer **16**.

With respect to the diffusion barrier dielectric layer **16** shown in FIG. **2**, the diffusion barrier dielectric layer **16** is formed from a silicon-rich silicon oxide dielectric material employing plasma enhanced chemical vapor deposition (PECVD) in accord with the following process: (1) silicon source gas silane (SiH_4); (2) carrier gases nitrogen, argon and helium; (3) power from about 100 to about 5000 watts;

(4) temperature from about 200 to about 400 degrees centigrade; and (5) pressure from about 1 milliTorr to about 100 Torr. Preferably the silicon rich silicon oxide diffusion barrier dielectric layer is formed to a thickness of from about 50 to about 5000 angstroms. The preferred degree of silicon enrichment of the silicon rich silicon oxide dielectric layer is obtained when the refractive index of the material is from about 1.47 to about 1.8.

Referring now more particularly to FIG. 3, there is shown a schematic cross-sectional drawing illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional drawing is shown in FIG. 2 in accord with the first preferred embodiment of the present invention. Shown in FIG. 3 is a microelectronics fabrication otherwise equivalent to the microelectronics fabrication shown in FIG. 2, but where there has been formed a patterned microelectronics conductive layer 20 to complete an inter-level metal (IMD) dielectric layer.

With respect to the patterned microelectronics conductive layer 20 shown in FIG. 3, the patterned microelectronics conductive layer 20 is selected from microelectronics conductor materials including but not limited to microelectronics metals, microelectronics conductive compounds, microelectronics alloys and microelectronics semiconductor materials, formed employing methods such as vacuum evaporation, chemical vapor deposition (CVD), physical vapor deposition (PVD) sputtering and electrodeposition (ED) methods, and patterned employing photolithographic methods and materials as are known in the art of microelectronics fabrication.

The present invention provides a method for forming an inter-level metal dielectric (IMD) layer comprising a dielectric layer and a conductive layer with an intermediate diffusion barrier dielectric layer between them to attenuate inter-diffusion.

Second Preferred Embodiment

FIG. 4 to FIG. 8 is a series of schematic cross-sectional diagrams illustrating the formation upon a semiconductor substrate employed within an integrated circuit microelectronics fabrication an inter-level metal dielectric (IMD) layer comprising a low dielectric constant dielectric layer having a diffusion barrier dielectric layer intermediate between it and a copper conductor layer FIG. 4 is a schematic cross-sectional diagram of an integrated circuit microelectronics fabrication at an early stage in its fabrication in accord with a more specific embodiment of the present invention which constitutes a second preferred embodiment of the present invention.

Shown in FIG. 4 is a semiconductor substrate 30 upon which is formed a patterned microelectronics layer 32 and a low dielectric constant dielectric layer 34.

With respect to the semiconductor substrate 30 showing in FIG. 4, the semiconductor substrate 30 is analogous to the substrate 10 shown in FIG. 1 of the first preferred embodiment of the present invention. Preferably the semiconductor substrate 30 is a silicon single crystal substrate of (100) crystalline orientation

With respect to the patterned microelectronics layer 32 shown in FIG. 4, the patterned microelectronics layer 32 is analogous to the patterned microelectronics layer 12 shown in FIG. 1 of the first preferred embodiment of the present invention.

With respect to the low dielectric constant dielectric layer 34 shown in FIG. 2, the low dielectric constant dielectric layer 34 is analogous to the dielectric layer 14 shown in FIG. 1 of the first preferred embodiment of the present invention. Preferably the low dielectric constant dielectric layer 34 is a fluorine-doped silicon oxide dielectric glass (FSG) material formed employing the following process: (1) silicon source gases silage (SiF_4) and tetrafluoromethane (SiF_4); (2) oxidizing gas O_2; (3) carrier gases helium and argon; (4) power from about 100 to about 5000 watts; (4) temperature form about 200 to about 400 degrees centigrade; and (5) pressure from about 1 milliTorr to about 100 Torr. Preferably the FSG layer is formed to a thickness of from about 100 to about 10,000 angstroms.

Referring now more particularly to FIG. 5, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the integrated circuit microelectronics fabrication whose schematic cross-sectional diagram is shown in FIG. 4 in accord with the second preferred embodiment of the present invention. Shown in FIG. 5 is an integrated circuit microelectronics fabrication otherwise equivalent to the integrated circuit microelectronics fabrication shown in FIG. 4, but where there has been formed over the semiconductor substrate a silicon rich silicon oxide diffusion barrier dielectric layer 36.

With respect to the silicon rich silicon oxide diffusion barrier dielectric layer 36, the silicon rich silicon oxide diffusion barrier layer 36 is equivalent or analogous to the diffusion barrier dielectric layer 16 shown in FIG. 2 of the first preferred embodiment of the present invention.

Referring now more particularly to FIG. 6, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the integrated circuit microelectronics fabrication shown in FIG. 5 in accord with the second preferred embodiment of the present invention. Shown in FIG. 6 is an integrated circuit microelectronics fabrication otherwise equivalent to the integrated circuit microelectronics fabrication shown in FIG. 5, but where there has been formed over the semiconductor substrate a second dielectric layer 38. Formed over the substrate is a patterned photoresist etch mask layer 40.

With respect to the dielectric layer 38 shown in FIG. 6, the dielectric layer 38 is a dielectric layer formed employing methods including but not limited to chemical vapor deposition (CVD) methods, plasma enhanced chemical vapor deposition methods (PECVD) methods, high density plasma chemical vapor deposition (HDP-CVD) methods, sub-atmospheric pressure thermal chemical vapor deposition (SACVD) methods, spin-on-glass (SOG) methods and spin-on-polymer (SOP) methods. Preferably the second dielectric layer is a silicon containing dielectric layer formed employing plasma enhanced chemical vapor deposition (PECVD) or, alternatively, formed employing high density plasma chemical vapor deposition (HDP-CVD).

Referring now more particularly to FIG. 7, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the integrated circuit microelectronics fabrication whose schematic cross-sectional diagram s shown in FIG. 6 in accord with the second preferred embodiment of the present invention. Shown in FIG. 7 is an integrated circuit microelectronics fabrication otherwise equivalent to the integrated circuit microelectronics fabrication shown in FIG. 6, but where there has been etched the pattern of the photoresist etch mask layer 40 through the dielectric layer 38' and the diffusion barrier dielectric layer 36' to the conductive layer 32, followed by stripping of the photoresist etch mask layer 40. The etched pattern 41 has been filled with a conductor layer 42.

With respect to the etching of the pattern 41 shown in FIG. 7, the etching of the pattern 41 employs materials and

methods suitable to the dielectric material of the dielectric layer **38** and diffusion layer **36**, as are known in the art of microelectronics fabrication. The stripping of the photoresist etch mask layer **40** after etching of the pattern **41** is accomplished employing methods and materials as are known in the art of microelectronics fabrication.

With respect to the conductor layer **42** shown in FIG. **7**, the conductor layer **42** is a copper metal or alloy layer formed employing methods including but not limited to vacuum evaporation, physical vapor deposition (PVD) sputtering and electrodeposition (ED) methods.

Referring now more particularly to FIG. **8**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the integrated circuit microelectronics fabrication whose schematic cross-sectional diagram is shown in FIG. **7**. Shown in FIG. **8** is an integrated circuit microelectronics fabrication otherwise equivalent to the integrated circuit microelectronics fabrication shown in FIG. **7**, but where there has been planarized **44** the surface of the dielectric layer **38"** and the copper layer **42'**.

With respect to the planarization **44** shown in FIG. **8**, the planarization **44** employs a chemical mechanical polish (CMP) planarization process as is known in the art of microelectronics fabrication.

The present invention provides a method for forming an inter-level metal dielectric (IMD) layer comprising a low dielectric constant dielectric layer, intermediate diffusion barrier dielectric layer and a copper conductor layer, with attenuated inter-diffusion of species between the dielectric layers and the copper layer.

Experimental

The benefits and advantages of the preferred embodiments of the present invention are exemplified by the results of experimental measurements performed upon samples fabricated in accord with the present invention. Dielectric layers were formed employing fluorine-doped, silicon containing glass (FSG) dielectric material deposited by HDP-CVD method on silicon semiconductor substrates of (100) orientation to a thickness of 1000 angstroms. Various dielectric materials were formed over the silicon semiconductor substrates and characterized by their composition and/or refractive indices as determined employing ellipsometric and reflectometric measurement methods. The silicon semiconductor substrate samples were treated to an alloying step for two hours at 400 degrees centigrade. The samples were then analysed by secondary ion mass spectrometry (SIMS) and by reflectance back scattering (RBS) methods. The results are shown in FIG. **9**, which illustrates the concentration of fluorine species as a function of depth of thickness of the FSG layer adjacent to the various dielectric layers. It can be seen that the diffusion of fluorine species into the silicon-rich silicon oxide dielectric layer is much less than into the other silicon oxide layers formed by PECVD, which are closer to stoichiometric silicon oxide based on the process conditions employed as determined by refractive index measurements. For comparison, the diffusion of fluorine species into silicon nitride and silicon oxynitride dielectric layers included in the sample group are also shown in FIG. **9**. These materials are known to be superior diffusion barrier materials, and it may be seen that the silicon rich silicon oxide dielectric layer is nearly as good a diffusion barrier as the layers formed from silicon nitride and silicon oxynitride dielectric materials.

As will be evident to a person skilled in the art, the preferred embodiments of the present invention are illustrative of the present invention rather than limiting of the present invention. Revisions and modifications may be made to the materials, structures and dimensions through which is provided the preferred embodiments of the present invention while still providing embodiments which are within the spirit and scope of the present invention, as defined by the appended claims.

What is claimed is:

1. A method for forming upon a substrate employed within a microelectronics fabrication an inter-level metal dielectric (IMD) layer comprising:

providing a substrate;

forming upon the substrate a patterned microelectronics layer;

forming over the substrate a dielectric layer;

forming over the dielectric layer a silicon rich silicon oxide diffusion barrier dielectric layer; and

forming over the substrate a patterned conductor layer.

2. The method of claim **1** wherein there is attenuated inter-diffusion between the dielectric layer and the conductor layer.

3. The method of claim **1** wherein the substrate is employed within a microelectronics fabrication selected from the group consisting of:

integrated circuit microelectronics fabrications;

charge coupled device microelectronics fabrications;

solar cell microelectronics fabrications;

optoelectronics microelectronics fabrications;

ceramic substrate microelectronics fabrications; and

flat panel display microelectronics fabrications.

4. The method of claim **1** wherein the patterned microelectronics layer is selected from the group consisting of:

microelectronics conductor layers;

microelectronics semiconductor layers; and

microelectronics dielectric layers.

5. The method of claim **1** wherein the dielectric layer is formed employing a fluorine-doped silicon containing and/or carbon-containing dielectric material.

6. The method of claim **1** wherein the diffusion barrier dielectric layer is formed employing plasma enhanced chemical vapor deposition (PECVD) of a silicon-rich silicon oxide dielectric material.

7. The method of claim **6** wherein the silicon rich silicon oxide dielectric diffusion barrier layer material has a refractive index of from about 1.47 to about 1.8.

8. The method of claim **1** wherein the patterned conductor layer is formed from copper or copper alloy conductor material.

9. A method for forming upon a semiconductor substrate employed within an integrated circuit microelectronics fabrication an inter-level metal dielectric (IMD) layer comprising:

providing a semiconductor substrate having formed therein a patterned microelectronics layer and a first dielectric layer employing fluorine-doped low dielectric constant dielectric material;

forming over the semiconductor substrate a silicon rich silicon oxide dielectric diffusion barrier layer;

forming over the substrate a second dielectric layer;

forming over the substrate a patterned photoresist etch mask layer and etching the pattern thereof into the second dielectric layer and diffusion barrier dielectric layer followed by stripping the photoresist etch mask layer;

filling the etched pattern with a copper conductor material; and

planarizing the surface of the second dielectric layer and copper layer.

10. The method of claim **9** wherein there is attenuated diffusion of fluorine species from the first low dielectric constant FSG layer into the silicon rich silicon oxide diffusion barrier dielectric layer.

11. The method of claim **9** wherein the semiconductor substrate is a silicon semiconductor substrate.

12. The method of claim **9** wherein the patterned microelectronics layer is formed from materials selected from the group consisting of:

microelectronics conductor materials;

microelectronics semiconductor materials; and

microelectronics dielectric materials.

13. The method of claim **9** wherein the first fluorine-containing low dielectric constant dielectric layer is formed from material selected from the group consisting of:

fluorine-doped silicon containing glass (FSG) dielectric material;

fluorine-containing carbon containing dielectric material; and

fluorine-containing carbon and/or silicon containing dielectric material.

14. The method of claim **9** wherein the silicon-rich silicon oxide dielectric layer is formed employing plasma enhanced chemical vapor deposition (PECVD).

15. The method of claim **14** wherein the silicon rich silicon oxide dielectric material has a refractive index of from about 1.47 to about 1.8.

16. The method of claim **9** wherein the second dielectric layer is formed employing dielectric material selected from the group consisting of:

silicon containing dielectric material;

fluorine-containing silicon containing glass dielectric material;

fluorine-containing carbon containing dielectric material; and

fluorine-containing carbon and silicon containing dielectric material.

17. The method of claim **9** wherein the copper containing conductor material is formed employing electrodeposition (ED) method.

18. The method of claim **9** wherein the planarization process is a chemical mechanical polish (CMP) planarization process.

* * * * *

Exhibit F

US006107206A

United States Patent [19]

Chao et al.

[11] Patent Number: 6,107,206

[45] Date of Patent: Aug. 22, 2000

[54] **METHOD FOR ETCHING SHALLOW TRENCHES IN A SEMICONDUCTOR BODY**

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[21] Appl. No.: **09/152,350**

[22] Filed: **Sep. 14, 1998**

[51] **Int. Cl.**[7] **H01L 21/302**; H01L 21/461

[52] **U.S. Cl.** **438/706**; 438/710; 438/719; 438/720; 438/721

[58] **Field of Search** 438/706, 724, 438/221, 432, 248, 710, 719, 720

[56] **References Cited**

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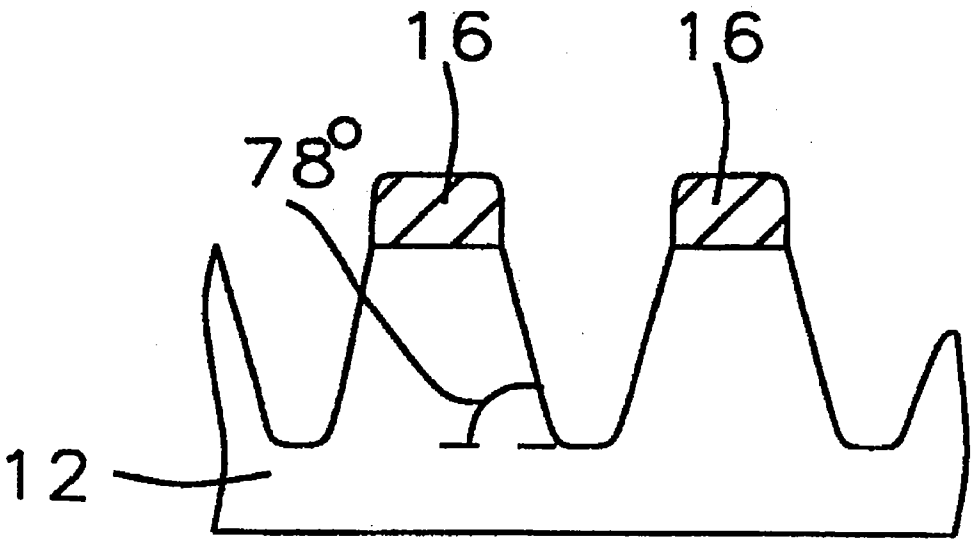
Primary Examiner—Richard Elms
Assistant Examiner—Michael S. Lebentritt
Attorney, Agent, or Firm—George O. Saile; Stephen B. Ackerman; Wolmar J. Stoffel

[57] **ABSTRACT**

A method of etching closely spaced trenches in a silicon body wherein a masked silicon body is introduced into a plasma etching apparatus. An object having an exposed silicon surface that is consumable by a plasma environment is provided in the apparatus. A reactive plasma environment is established in the apparatus which removes silicon from the body and the silicon object. The additional silicon from the object in the plasma influences the silicon removal from the body to thereby provide tapered trench side walls.

20 Claims, 2 Drawing Sheets



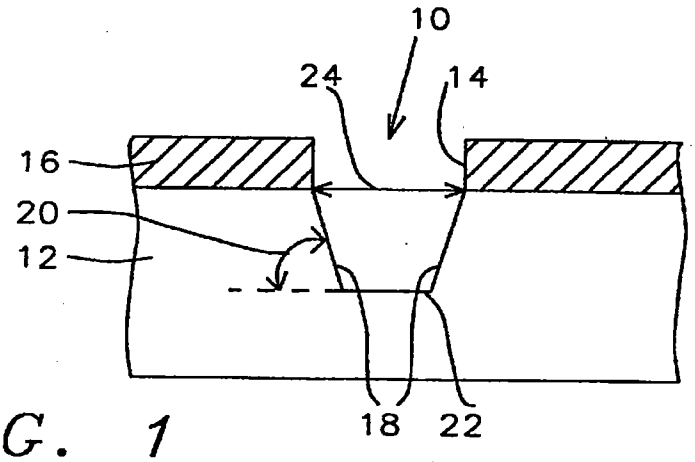


FIG. 1

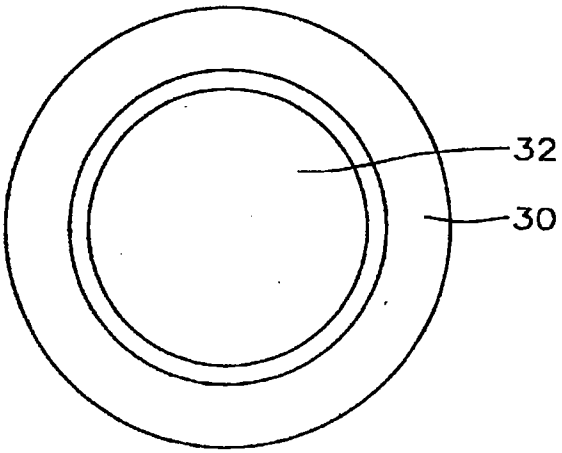


FIG. 2

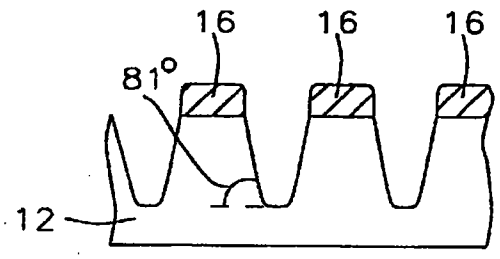


FIG. 3a

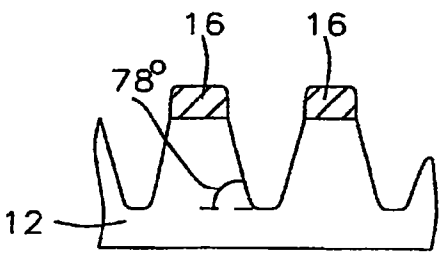


FIG. 3b

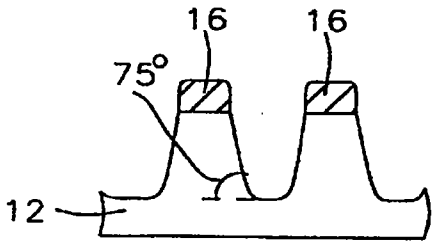


FIG. 3c

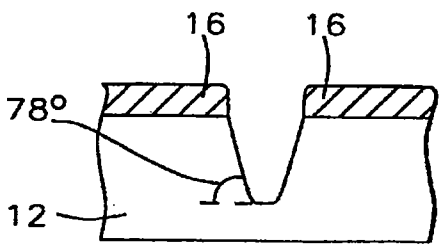


FIG. 4a

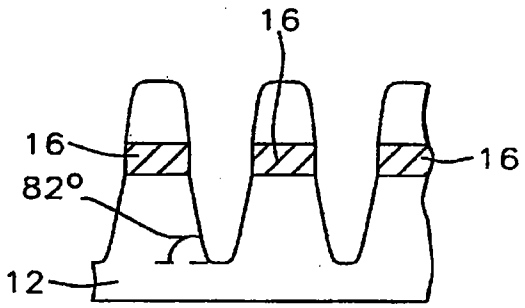


FIG. 4b

METHOD FOR ETCHING SHALLOW TRENCHES IN A SEMICONDUCTOR BODY

BACKGROUND OF THE INVENTION

The invention relates to fabrication of semiconductor devices, more particularly to the etching of shallow isolation trenches in monocrystalline silicon substrates.

The fabrication of trenches in semiconductor substrates of integrated circuit devices that have an aspect ratio (depth to width ratio) greater than 1 to 1 is useful in several areas of ULSI (ultra large scale integration) processing. Trench etch processing has become critical to the fabrication of state-of-art electronic devices exploiting three dimensional structural concepts such as trench capacitors, trench isolation, and trench transistors.

Currently, shallow trench isolation (STI) uses Cl_2/HBr reactive ion etching to form trenches in masked monocrystalline silicon substrates. The trenches most desirably have smooth planar trench walls that slope inwardly in order to avoid void formations in the materials used to fill the trenches. The trenches are normally filled using chemical vapor deposition refill operations. Desirably, the slope of the trench walls will be less than approximately 85 degrees to avoid void formations, and greater than 75 degrees to conserve area on the device. The trench wall slope is defined as the complementary angle of the angle between the trench wall and the horizontal flat trench floor.

As the semiconductor devices become more microminiturized, the isolation trenches have become smaller and more narrow. This microminiturization resulted in serious problems in controlling the trench wall slope and the planarity of the walls.

Various methods and etching apparatus are known for controlling the profile and shape of etched trenches in semiconductor bodies. U.S. Pat. No. 5,298,790 discloses an etching process wherein and etching mask, which includes a layer of polysilicon that will absorb non-vertically traveling ions, is provided to influence the resultant trench profile. U.S. Pat. No. 4,690,729 discloses a method for etching trenches in a silicon body wherein an enchant mask is provided that includes silicon oxides. During etching, the silicon oxides of the mask are deposited on the resultant trench side walls and influence the etching action. U.S. Pat. No. 4,855,017 discloses a method for etching trenches in a silicon body. In the method, material is selectively deposited on the trench side walls during etching by including various agents in the plasma that will react with the silicon and form etch products that deposit on the trench walls. These deposits influences the etching action of the plasma to form the desired trench profile. U.S. Pat. No. 5,707,486 discloses a plasma reactor for etching various materials. The reactor has an electrode structure that defines the plasma generating field.

SUMMARY OF THE INVENTION

An object of the invention is to decrease the etching profile angle for small trench etching.

Another object of the invention is to provide a method to decrease the etching profile angle for low clear ratio [(1-Mask cover area)/(total wafer area)] shallow trench etching.

Yet another object of the invention is to provide an etching method for forming shallow isolation trenches wherein the etching profile angle can be controlled.

Still another object of the invention is to provide a reactive ion etching method wherein the profile angle of the trench wall can be controlled when the trenches are very narrow and/or the clear ratio is low.

The present invention is a method for etching closely spaced trenches in a silicon body, which trenches have sloping side walls. In the method, a silicon body, with a surface masking layer with openings that define closely spaced isolation trenches, is introduced into a plasma etching apparatus. A silicon object having an exposed silicon surface that is consumable in a plasma environment is provided within the apparatus. A reactive plasma environment is established within the apparatus that removes silicon from the silicon body through the mask openings, and silicon from the silicon object. The silicon from the object influences the silicon removed from the body thereby resulting in tapered side walls on the resultant trenches.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described with reference to the accompanying drawings, wherein:

FIG. **1** is a profile view of a typical trench, in greatly enlarged scale, used in the fabrication of trench isolation structures for semiconductor devices.

FIG. **2** shows a substrate support **30** that supports a wafer **32** on its top surface.

FIGS. **3***a*, **3***b*, and **3***c* are profile views of trenches that are associated with examples in the specification.

FIGS. **4***a*, and **4***b* are profile views of trenches that are associated with examples in the specification.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is a method for controlling the slope of a trench wall during a reactive ion etching process in the fabrication of very small semiconductor devices utilizing filled trench isolation. Referring to FIG. **1**, there is illustrated a trench **10** that has been etched into a monocrystalline silicon substrate **12** through an opening **14** in mask **16**. As indicated, the side walls slope inwardly forming a tapered trench. In semiconductor processing, a trench with sloping side walls can be filled with an insulating material, usually using CVD processes, with less probability of forming voids in the insulating material. Also, the trench walls should be flat, without an undercut beneath the edges of the mask. However, if the slope of the trench side walls is too great, the isolation trenches will take up too much area on the device surface. The slope of the side walls is indicated by angle **20** in FIG. **1**, as the complimentary angle of the angle formed by the side wall **18**, and trench bottom surface **22**. A trench with vertical side walls will have a slope of 90 degrees. A trench with tapered side walls will have a slope less than 90 degrees. A trench for a trench isolation structure will preferably have a slope in the range of 70 to 85 degrees.

It has been discovered that as the size of the device geometry gets increasingly smaller, the slope of the trench walls, produced by reactive ion etching gets greater, approaching the vertical. The factors that affect the trench wall slope have been discovered to be (1) the width of the trenches, and (2) the pattern density of the mask used to form the trenches. The trench width is indicated in FIG. **1** as the dimension **24**, The pattern density D is given by the formula D=(photoresist mask cover area)/(total wafer area). It has been discovered that in order to produce microminiturized trenches with walls having a slope in the range of 70° to 85° the trench width must be in the range of 0.3 μm and below, when the clear ratio (% of surface not covered by photoresist) is less than 60%.

As is illustrated by the Examples 1 and 2 that follow, the etching profile angle of the trench walls depends on the trench width and the clear ratio. Since silicon is believed to be the source of passivation that generates the taper etching profile, we propose to add consumable silicon in the etching chamber to increase the passivation source for trench etching for small trench widths and spacing, and low clear ratio applications.

Referring now to FIG. 2, there is illustrated a method and structure for increasing the silicon during etching. FIG. 2 shows a substrate support **30** that supports a wafer **32** on its top surface. Support **30** can be formed of silicon, or more conveniently be formed of glass with a surface layer of polysilicon. The wafer **32** can be secured to the support **30** if desired, possibly with electrostatic techniques.

EXAMPLE 1

Three monocrystalline silicon substrates were each masked with a photoresist layer. The layers were all exposed and cured to form trench openings of various widths. The first mask layer openings were 0.30 um in width. The second mask layer openings were 0.35 um in width. The third mask layer openings 0.40 um in width. All of the substrates were reactive ion etched in a reactive plasma environment defined as follows:

50 mT/900 w 30 G/100 HBr 10 Cl_2 40 HeO_2 15 CF_4/10 s

80 mT/900 w 30 G/100 HBr 10 Cl_2 40 HeO_2 15 CF_4/10 s

100 mT/900 w 30 G/100 HBr 10 Cl_2 40 HeO_2 15 CF_4/10 s

(note: HeO_2 is O_2 diluted in He—to enable good control of low O_2 flow rate)

The substrates were removed from the apparatus, and sectioned to reveal the trench profiles. The first substrate trenches, with a width of 0.30 um, had walls with a slope of 81 degrees. The second substrate trenches, with a width of 0.35 um, had walls with a slope of 78 degrees. The third substrate trenches, with a width of 0.40 um had a slope of 75 degrees. The depth of the trenches was 3.5 K Å. The pattern density of the masks were approximately the same, on the order of 70%. These results indicate that as the trench widths increase, the slope of trench wall increases. This example illustrates the problem facing the semiconductor industry, i.e. the increasing of trench wall slope as the geometry becomes smaller.

EXAMPLE 2

Two monocrystalline silicon substrates were masked with a masking layer that defined trenches of approximately equal width. The pattern of the openings on the first substrate had a clear ratio of 65%. The clear ratio on the second wafer was 50%. The trench width on both wafers was 0.40 um. The substrates were placed in a reactive ion etch apparatus and exposed to a reactive plasma environment defined as follows:

50 mT/800 w 30 g/100 HBr 20 Cl_2 30 HeO_2 20 CF_4/8 s

80 mT/750 w 30 g/100 Br 20 Cl_2 30 HeO_2 20 CF_4/8 s

100 mT/750 w 30 g/100 HBr 20 Cl_2 30 HeO_2 20 CF_4/44 s

The substrates were removed and sectioned, as in Example 1. The first substrate trenches, with a clear ratio of 65%, had a slope of 78 degrees. The second substrate trenches, with a clear ratio (% of surface covered by photoresist or [(1-mask cover area)/total wafer area]) of 50%, had a slope of 82 degrees. This Example illustrates that as the clear ratio is decreased, the slope of the trench walls increase.

EXAMPLE 3

Three substrates are masked as in Example 1, using the same mask with similar sized openings. The substrates are placed in a reactive etching apparatus, as in Example 1 but with the substrates placed on a substrate holder, made of glass, with a coating layer of polycrystalline silicon. The substrate holder is indicated in FIG. 2, and has an exposed silicon surface area on approximately 140 cm^2. The reactive plasma is similar to the one described in Example 1. After the etching was complete and the substrates sectioned, the following results is obtained.

	Trench Width	Slope	Slope as in Ex. 1
#1 Substrate	0.30 μm	78°	81 degree
#2 Substrate	0.35 μm	75°	78 degree
#3 Substrate	0.40 μm	72°	75 degree

The above comparison illustrates the advantages of the invention.

While preferred embodiments of the present invention and their advantages have been set out in the above description, the invention is no limited thereto, but only by the spirit and scope of the appended claims.

We claim:

1. A method of etching closely spaced trenches in a silicon body, said trenches having sloping side walls, the method comprising,

introducing a monocrystalline silicon semiconductor body, with a surface masking layer with openings that define closely spaced shallow isolation trenches, into a plasma etching apparatus,

providing a silicon object having an exposed silicon surface that is consumable by a plasma environment within the apparatus,

establishing a reactive plasma environment within the apparatus that removes silicon from the semiconductor body through said openings in said masking layer and also silicon from said silicon object, said plasma influenced by the silicon removed from said object to thereby provide tapered side walls in the resultant trenches.

2. The method of claim **1** wherein said openings have a width less than 0.30 μm.

3. The method of claim **2** wherein said openings have a width in the range of 0.2 to 0.3 μm.

4. The method of claim **1** wherein said masking layer has a clear ratio, defined by [1-(photo resist cover area)/(total wafer area)] that is less than 60%.

5. The method of claim **4** wherein said clear ratio is in the range of 10% to 60%.

6. The method of claim **1** wherein said silicon object is a wafer support holder having a peripheral area surrounding said semiconductor body that has at least a surface layer of silicon.

7. The method of claim **6** wherein said silicon object is formed of glass with a layer of polycrystalline silicon on the surface.

8. The method of claim **6** wherein the ratio of the surface area of the wafer to the peripheral surface area of the silicon object is in the range of 0.5 to 1.0.

9. The method of claim 2 wherein the slope of the resultant side walls of the trenches is less than 85 degrees.

10. The method of claim 9 wherein the slope range of the resultant side walls of the trenches is in the range of 70 to 85 degrees.

11. The method of claim 1 wherein said etching is achieved with a plasma environment which includes HBr, Cl_2, He, O_2, and CF_4.

12. The method of claim 11 wherein an electric field is established within the etching apparatus that has its axis perpendicular to the surface plane of the semiconductor body.

13. The method of claim 2 wherein the masking layer has a clear ratio that is less than 60% resulting in a trench wall slope that is less than 85 degrees.

14. A method of etching closely spaced trenches in a silicon body, said trenches having sloping side walls, the method comprising,

introducing a monocrystalline silicon semiconductor body, with a surface masking layer with openings that define closely spaced shallow isolation trenches, into a plasma etching apparatus,

providing a silicon object having an exposed silicon surface that is consumable by a plasma environment within the apparatus,

establishing a reactive plasma environment within the apparatus that removes silicon from the semiconductor body through said openings in said masking layer and also silicon from said silicon object, said plasma influenced by the silicon removed from said object to thereby provide tapered side walls in the resultant trenches; and

said surface masking layer has a clear ratio that is less than 60% resulting in a trench wall slope that is less than 85 degrees.

15. The method of claim 14 wherein said openings have a width less than 0.30 μm; and the slope of the resultant side walls of the trenches is less than 85 degrees.

16. The method of claim 14 wherein said openings have a width in the range of 0.2 to 0.3 μm.

17. The method of claim 14 wherein said masking layer has a clear ratio, defined by [1-(photo resist cover area)/(total wafer area)] that is in the range of 10% to 60%.

18. The method of claim 14 wherein said silicon object is a wafer support holder having a peripheral area surrounding said semiconductor body that has at least a surface layer of silicon; the ratio of the surface area of the wafer to the peripheral surface area of the silicon object is in the range of 0.5 to 1.0.

19. The method of claim 18 wherein said silicon object is formed of glass with a layer of polycrystalline silicon on the surface.

20. The method of claim 14 wherein said etching is achieved with a plasma environment which includes HBr, Cl_2, He, O_2, and CF; and an electric field is established within the etching apparatus that has its axis perpendicular to the surface plane of the semiconductor body.

* * * * *